WHAT IS CLAIMED IS:

1. A redundancy fuse circuit for replacing a defective cell in a memory cell array with a redundancy column, comprising:

a fuse circuit in which an address of the defective cell or a block including the defective cell is programmed as a defective address by presence/absence of cut-off of a fuse device;

a data latch circuit which latches a signal supplied from a tester to program the defective address in a dummy manner; and

a comparator which replaces the defective cell with the redundancy cell based on an address signal supplied from the tester and an output signal of the data latch circuit at a test time of the redundancy fuse circuit.

2. The redundancy fuse circuit according to claim 1, wherein the memory cell array comprises a redundancy row including the redundancy cell, and the defective address is a defective row address or an address of a block including the defective row.

3. The redundancy fuse circuit according to claim 1, wherein the memory cell array comprises a redundancy column including the redundancy cell, and the defective address is a defective column address or an address of a block including the defective column.

4. The redundancy fuse circuit according to

claim 1, further comprising:

a logic circuit which supplies the output signal of the data latch circuit to the comparator at the test time and which supplies the output signal of the fuse circuit to the comparator at a usual operation time.

5. The redundancy fuse circuit according to claim 1, wherein the fuse device is of a type that is cut by laser.

6. The redundancy fuse circuit according to claim 1, wherein the fuse device is an electric fuse capable of being electrically cut off.

7. A semiconductor memory comprising the redundancy fuse circuit according to claim 1.

8. An integrated system comprising the semiconductor memory according to claim 7.

9. A memory embedded microcomputer comprising the redundancy fuse circuit according to claim 1.

10. An integrated system comprising the memory embedded microcomputer according to claim 9.

11. A semiconductor integrated circuit comprising the redundancy fuse circuit according to claim 1.

12. An integrated system comprising the semiconductor integrated circuit according to claim 11.

13. A test method of a redundancy fuse circuit for replacing a defective cell in a memory cell array with a redundancy column, comprising:

latching a signal supplied from a tester in a data

latch circuit to perform dummy programming of a defective address; and

comparing an address signal supplied from the tester with an output signal of the data latch circuit to determine whether or not the defective cell is replaced with the redundancy cell at a test time of the redundancy fuse circuit.

14. The test method according to claim 13, further comprising:

cutting off a fuse device in the fuse circuit after finishing the test.

15. The test method according to claim 13, wherein the defective address is a defective row address or an address of a block including a defective row.

16. The test method according to claim 13, wherein the defective address is a defective column address or an address of a block including a defective column.

17. The test method according to claim 13, further comprising:

supplying the output signal of the data latch circuit to the comparator at the test time, and supplying the output signal of the fuse circuit to the comparator at a usual operation time.

18. The test method according to claim 17, wherein the fuse device in the fuse circuit is of a type that is cut by laser.

19. The test method according to claim 17, wherein

the fuse device in the fuse circuit is an electric fuse capable of being electrically cut off.

20. The test method according to claim 13, further comprising:

treating the circuit as inferior goods without cutting off any fuse device in a case where the test results in NG.